AMENDMENTS TO THE SPECIFICATION

On page 11, please amend the first full paragraph as follows:

In the second example, a current of the current source I1 is split into collector currents of transistors Q2 and Q3 according to a voltage difference between the input voltage VIN and the reference and the reference voltage V1. A collector current of the transistor Q2 is further split into a collector current of the transistor Q7 and a collector current (a first control current) of the transistor Q8 according to a voltage difference between a voltage at the output VOUT (an inter-terminal voltage between the collector and emitter of the output transistor Q1) and the reference voltage V3. The above workings in the second example are the same as in the first example. Furthermore, a collector current (a second control ~~circuit~~current) of the transistor Q10 obtained by amplification of the first control current in an amplifier constituted of a second current mirror circuit is provided by further splitting a collector current of the transistor Q7.

On page 11, please amend the second full paragraph as follows:

As a result, a base current is extracted from the base of the transistor Q1 using the second control current obtained by amplifying the first control ~~circuit~~current flowing into the transistor Q8 when a voltage at the output VOUT takes a voltage in the vicinity of the reference voltage V3, thereby enabling a collector current of the output transistor Q1 to be reduced more efficiently than in the first example. Furthermore, if a base current of the output transistor Q1 is extracted after amplified at a larger mirror ratio in the second current mirror circuit, increase occurs in current amount extracted from the base of the output transistor Q1 when a voltage at the output OUT falls to a value lower than the reference voltage V3, thereby enabling falling in voltage at the output VOUT to be suppressed at a higher speed.